AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-5 (Cancelled)

6. (Currently Amended) A nonvolatile semiconductor memory comprising:

(a) a memory cell comprising second semiconductor regions for a source and a drain, respectively, formed in a first semiconductor region in a semiconductor substrate; a charge accumulation layer formed on a region between said second semiconductor regions for the source and the drain, through a gate insulating film; and a control electrode provided on said charge accumulation layer through an insulating film;

(b) a third semiconductor region formed between said first semiconductor region and the semiconductor substrate;

(c) first voltage application means for applying a voltage to said control electrode;

(d) a second voltage application means for applying a voltage to said first semiconductor region; and

(e) a third voltage application means for applying a voltage to said third semiconductor region; and

(f) means for determining a threshold voltage of said memory cell,

wherein a first voltage is applied to said control electrode and a second voltage is applied to said first semiconductor region during a first period, thereby allowing electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region,

the threshold voltage of said memory cell is determined in a second period following said first period,

if it is determined that the threshold voltage of said memory cell is higher than a predetermined threshold voltage, the first voltage is applied to said control electrode and the second voltage is applied to said first semiconductor region in a third period following said second period, thereby allowing the electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region, and

a third voltage is applied to said third semiconductor region during said first to third periods.

7. (Original) A nonvolatile semiconductor memory according to claim 6, wherein

a first voltage is applied to the control electrode of said nonvolatile semiconductor memory, and a second voltage is applied to said first semiconductor region; and

a potential difference between said first voltage and said second voltage corresponds to a voltage allowing electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region.

8. (Original) A nonvolatile semiconductor memory according to claim 6, wherein

a first voltage is applied to the control electrode of said nonvolatile semiconductor memory, and a second voltage is applied to said first semiconductor region; and

a potential difference between said first voltage and said second voltage corresponds to a voltage allowing electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region by a tunnel phenomenon.

9. (Currently Amended) A nonvolatile semiconductor memory according to claim 6, wherein

a first voltage is applied to the control ~~section~~ electrode of said nonvolatile semiconductor memory, a second voltage is applied to said first semiconductor region, and a third voltage is applied to said third semiconductor region; and

said third voltage is higher than said second voltage.

10. (Original) A nonvolatile semiconductor memory according to claim 6, wherein

said nonvolatile semiconductor memory applies a first voltage to said control electrode, and applies a second voltage to said first semiconductor region, thereby pulling out electrons accumulated in said charge accumulation layer into said first semiconductor region, to thereby allow data to be electrically deleted.

11. (Original) A nonvolatile semiconductor memory according to claim 6, wherein

said nonvolatile semiconductor memory comprises a plurality of memory cell groups each having a plurality of

said memory cells formed therein, and the memory cells in each memory cell group are formed above a non-separated third semiconductor region.

12. (Original) A nonvolatile semiconductor memory according to claim 6, wherein

said nonvolatile semiconductor memory comprises a plurality of memory cell groups each having a plurality of said memory cells formed therein, and the memory cells in each memory cell group are formed above a third semiconductor region separated at intervals of units of a predetermined number of the memory cells.

13. (Original) A nonvolatile semiconductor memory according to claim 6, wherein

said nonvolatile semiconductor memory comprises a plurality of first memory cell groups each having a plurality of said memory cells in units of a first predetermined number of the memory cells; and a plurality of second memory cell groups each having said memory cells in units of a second predetermined number of the memory cells, the second predetermined number being higher than said first predetermined number;

the memory cells in said plurality of first memory cell groups are formed above a third semiconductor region separated at intervals of units of a third predetermined number of the memory cells; and

the memory cells in said plurality of second memory cell groups are formed above the third semiconductor region separated at intervals of units of a fourth predetermined number of the memory cells, the fourth predetermined number being higher than the third predetermined number.

Claims 14-17 (Cancelled)

18. (Original) A data deletion method for a nonvolatile semiconductor memory, the nonvolatile semiconductor memory comprising:

a memory cell comprising second semiconductor regions for a source and a drain, respectively, formed in a first semiconductor region in a semiconductor substrate; a charge accumulation layer formed on a region between said second semiconductor regions for the source and the drain through a gate insulating film; and a control electrode provided on said charge accumulation layer through an insulating film; and

a third semiconductor region formed between said first semiconductor region and the semiconductor substrate, wherein

the data deletion method comprising the steps of:

applying a first voltage to said control electrode, applying a second voltage to said first semiconductor region, and pulling out electrons accumulated in said charge accumulation layer into said first semiconductor region based on a potential difference between said first voltage and said second voltage in a first period;

determining a threshold voltage of said memory cell in a second period following said first period; and

applying the first voltage to said control electrode, applying the second voltage to said first semiconductor region and thereby pulling out the electrons accumulated in said charge accumulation layer into said first semiconductor region in a third period following said second period if the threshold voltage of said memory cell is higher than a predetermined threshold voltage, and wherein

a third voltage is applied to said third semiconductor region during said first to third periods.

19. (Original) A data deletion method for a nonvolatile semiconductor memory, according to claim 18, wherein

said third voltage is higher than said second voltage.

20. (Currently Amended) A nonvolatile semiconductor memory comprising:

(a) a memory cell comprising second semiconductor regions for a source and a drain, respectively, formed in a first semiconductor region in a semiconductor substrate; a charge accumulation layer formed on a region between said second semiconductor regions for the source and the drain through a gate insulating film; and a control electrode provided on said charge accumulation layer through an insulating film;

(b) a third semiconductor region (NiSO) formed between said first semiconductor region and the semiconductor substrate;

(c) first means for applying a voltage to said control electrode;

(d) second means for applying a voltage to said first semiconductor region; and

(e) third means for prohibiting a voltage from being

applied to said third semiconductor region; and

(f) means for determining a threshold voltage of said memory cell,

wherein the conductive type of said first semiconductor region is a p type and that of said third semiconductor region is an n type,

a first voltage is applied to said control electrode and a second voltage is applied to said first semiconductor region in a first period, thereby allowing electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region,

the threshold voltage of said memory cell is determined in a second period following said first period,

if it is determined that the threshold voltage of said memory cell is higher than a predetermined threshold voltage, the first voltage is applied to said control electrode and the second voltage is applied to said first semiconductor region in a third period following said second period, thereby allowing the electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region,

a second voltage is applied to said first semiconductor region in said first period and thereby said

third semiconductor region is charged through said first semiconductor region up to said second voltage, and

said third semiconductor region is maintained in a floating state during said first to third periods.

21. (Original) A nonvolatile semiconductor memory according to claim 20, wherein

a first voltage is applied to the control electrode of said nonvolatile semiconductor memory, and a second voltage is applied to said first semiconductor region; and

a potential difference between said first voltage and said second voltage corresponds to a voltage allowing electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region.

22. (Original) A nonvolatile semiconductor memory according to claim 20, wherein

a first voltage is applied to the control electrode of said nonvolatile semiconductor memory, and a second voltage is applied to said first semiconductor region; and

a potential difference between said first voltage and said second voltage corresponds to a voltage allowing electrons accumulated in said charge accumulation lay r to

be pulled out into said first semiconductor region by a tunnel phenomenon.

23. (Original) A nonvolatile semiconductor memory according to claim 20, wherein

a first voltage is applied to the control electrode of said nonvolatile semiconductor memory by said first means; a second voltage is applied to said first semiconductor region by said second means; and said third semiconductor region is maintained in a floating state by said third means.

24. (Original) A nonvolatile semiconductor memory according to claim 20, wherein

said nonvolatile semiconductor memory applies a first voltage to said control electrode, and applies a second voltage to said first semiconductor region, thereby pulling out electrons accumulated in said charge accumulation layer into said first semiconductor region, to thereby allow data to be electrically deleted.

25. (Original) A nonvolatile semiconductor memory according to claim 20, wherein

said nonvolatile semiconductor memory comprises a plurality of memory cell groups each having a plurality of said memory cells formed therein, and the memory cells in each memory cell group are formed above a non-separated third semiconductor region.

26. (Original) A nonvolatile semiconductor memory according to claim 20, wherein

said nonvolatile semiconductor memory comprises a plurality of memory cell groups each having a plurality of said memory cells formed therein, and the memory cells in each memory cell group are formed above a third semiconductor region separated at intervals of units of a predetermined number of the memory cells.

27. (Original) A nonvolatile semiconductor memory according to claim 20, wherein

said nonvolatile semiconductor memory comprises a plurality of first memory cell groups each having a plurality of said memory cells in units of a first

predetermined number of the memory cells; and a plurality of second memory cell groups each having said memory cells in units of a second predetermined number of the memory cells, the second predetermined number being higher than said first predetermined number;

the memory cells in said plurality of first memory cell groups are formed above a third semiconductor region separated at intervals of units of a third predetermined number of the memory cells; and

said first semiconductor region having the memory cells in said plurality of second memory cell groups formed therein is formed in the third semiconductor region separated at intervals of units of a fourth predetermined number of the memory cells, the fourth predetermined number being higher than the third predetermined number.

Claims 28-30 (Cancelled)

31. (Currently Amended) A data deletion method for a nonvolatile semiconductor memory, the nonvolatile semiconductor memory comprising:

a memory cell comprising second semiconductor regions for a source and a drain, respectively, formed in a first

semiconductor region in a semiconductor substrate; a charge accumulation layer formed on a region between said second semiconductor regions for the source and the drain through a gate insulating film; and a control electrode provided on said charge accumulation layer through an insulating film; and

a third semiconductor region formed between said first semiconductor region and the semiconductor substrate, wherein

the data deletion method comprises the steps of:

applying a first voltage to said control electrode, applying a second voltage to said first semiconductor region, and pulling out electrons accumulated in said charge accumulation layer into said first semiconductor region based on a potential difference between said first voltage and said second voltage in a first period;

determining a threshold voltage of said memory cell in a second period following said first period; and

applying the first voltage to said control electrode, applying the second voltage to said first semiconductor region and thereby pulling out the electrons accumulated in said charge accumulation layer, into said first semiconductor region in a third period following said

second period if the threshold voltage of said memory cell is higher than a predetermined threshold voltage, and wherein

the conductive type of said first semiconductor region is a p type and that of said third semiconductor region is an n type,

a second voltage is applied to said first semiconductor region in said first period and thereby said third semiconductor region is charged through said first semiconductor region up to said second voltage, and

said third semiconductor region is maintained in a floating state during said first to third periods.

32. (Original) A nonvolatile semiconductor memory comprising:

(a) a plurality of memory cell groups each having a plurality of memory cells formed on a main surface of a first semiconductor region in a semiconductor substrate, each memory cell comprising second semiconductor regions for a source and a drain, respectively, formed in said first semiconductor region; a charge accumulation layer formed on a region between the second semiconductor regions for the source and the drain through a gate insulating

film; and a control electrode provided on said charge accumulation layer through an insulating film;

(b) a third semiconductor region formed between said first semiconductor region and the semiconductor substrate;

(c) first voltage application means for applying a voltage to said control electrode; and

(d) second voltage application means for applying a voltage to said first semiconductor region and said third semiconductor region, respectively, wherein

said third semiconductor region is separated at intervals of units of a predetermined number of the memory cells in the plurality of memory cell groups.

33. (Original) A nonvolatile semiconductor memory according to claim 32, wherein

a first voltage is applied to the control electrode of said nonvolatile semiconductor memory, and a second voltage is applied to said first semiconductor region and said third semiconductor region, respectively; and

a potential difference between said first voltage and said second voltage corresponds to a voltage allowing electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region.

34. (Original) A nonvolatile semiconductor memory according to claim 32, wherein

a first voltage is applied to the control electrode of said nonvolatile semiconductor memory, and a second voltage is applied to said first semiconductor region and said third semiconductor region, respectively; and

a potential difference between said first voltage and said second voltage corresponds to a voltage allowing electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region by a tunnel phenomenon.

35. (Original) A nonvolatile semiconductor memory according to claim 32, wherein

said plurality of memory cell groups comprise a plurality of first memory cell groups each having a plurality of said memory cells in units of a first predetermined number of the memory cells; and a plurality of second memory cell groups each having said memory cells in units of a second predetermined number of the memory cells, the second predetermined number being higher than said first predetermined number;

the memory cells in said plurality of first memory cell groups are formed above a third semiconductor region separated at intervals of units of a third predetermined number of the memory cells; and

the memory cells in said plurality of second memory cell groups are formed above the third semiconductor region separated at intervals of units of a fourth predetermined number of the memory cells, the fourth predetermined number being higher than the third predetermined number.

Claims 36-38 (Cancelled)